Claims

We claim:

1. A method for forming an electronic structure, comprising the steps of:

providing a substrate; and

soldering a lead-free solder member to the substrate without using a joining solder to effectuate the soldering, wherein the solder member comprises a tin-antimony alloy that includes about 3% to about 15% antimony by weight.

2. The method of claim 1, wherein the tin-antimony alloy includes about 5% to about 10% antimony by weight.

3. The method of claim 1, wherein the soldering step includes reflowing the solder member.

4. The method of claim 1, wherein the soldering step reduces a height of the solder member between about 25% and about 30%.

5. The method of claim 1, wherein the substrate includes a ceramic ball grid array (CBGA) module or a plastic ball grid array (PBGA) module.

6. The method of claim 1, wherein the substrate includes a semiconductor chip.

7. A method for forming an electronic structure, comprising the steps of:

providing a first substrate and a second substrate;

soldering a lead-free solder member to the first substrate without using a joining solder to effectuate the soldering, wherein the solder member comprises a tin-antimony alloy that includes about 3% to about 15% antimony by weight; and

soldering the solder member to the second substrate with a lead-free joiner solder.

8. The method of claim 7, wherein the tin-antimony alloy includes about 5% to about 10% antimony by weight.

9. The method of claim 7, wherein the step of soldering the solder member to the second substrate includes reflowing the joiner solder at a temperature above a liquidus temperature of the joiner solder and below a highest temperature which will not damage any portion of the electronic structure.

10. The method of claim 7, wherein the step of soldering the solder member to the second substrate includes reflowing the joiner solder at a temperature above a liquidus temperature of the joiner solder and below about 250 °C.

11. The method of claim 7, wherein the step of soldering the solder member to the second substrate includes reflowing the joiner solder at a temperature above a liquidus temperature of the joiner solder and below a highest temperature which will not damage any portion of the electronic structure.

12. The method of claim 7, wherein the joiner solder comprises a tin-silver-copper alloy that includes by weight about 95.5-96.0% tin, about 3.5-4.0% silver, and about 0.5-1.0% copper.

13. The method of claim 12, wherein the step of soldering the solder member to the second substrate includes reflowing the joiner solder at a temperature between about 230 °C and about 250 °C.

14. The method of claim 7, wherein the step of soldering the solder member to the second substrate includes melting the solder member.

15. The method of claim 14, wherein the step of soldering the solder member to the second substrate includes intermixing the tin-antimony alloy with the joiner solder.

16. The method of claim 7, wherein the step of soldering the solder member to the second substrate does not include melting the solder member.

17. The method of claim 16, wherein the step of soldering the solder member to the second substrate does not include intermixing the tin-antimony alloy with the joiner solder.

18. The method of claim 7, wherein the first substrate includes a ceramic ball grid array (CBGA) module or a plastic ball grid array (PBGA) module.

19. The method of claim 7, wherein the first substrate includes a semiconductor chip.

20. An electronic structure, comprising:

a substrate;

a lead-free solder member soldered to the substrate with no joining solder between the solder member and the substrate, wherein the solder member comprises a tin-antimony alloy that includes about 3% to about 15% antimony by weight.

21. The electronic structure of claim 20, wherein the tin-antimony alloy includes about 5% to about 10% antimony by weight.

22. The electronic structure of claim 20, wherein the substrate includes a ceramic ball grid array (CBGA) module or a plastic ball grid array (PBGA) module.

23. The electronic structure of claim 20, wherein the substrate includes a semiconductor chip.

24. An electronic structure, comprising:

a first substrate;

a second substrate; and

a lead-free solder member soldered to the first substrate with no joining solder between the solder member and the first substrate, wherein the solder member comprises a tin-antimony alloy that includes about 3% to about 15% antimony by weight, and wherein the solder member is soldered to the second substrate with a lead-free joiner solder.

25. The electronic structure of claim 20, wherein the tin-antimony alloy includes about 5% to about 10% antimony by weight.

26. The electronic structure of claim 20, wherein the tin-antimony alloy is intermixed with the joiner solder.

27. The electronic structure of claim 20, wherein the tin-antimony alloy is not intermixed with the joiner solder.

28. The electronic structure of claim 20, wherein the joiner solder comprises a tin-silver-copper alloy that includes by weight about 95.5-96.0% tin, about 3.5-4.0% silver, and about 0.5-1.0% copper.

29. The electronic structure of claim 24, wherein the first substrate includes a ceramic ball grid array (CBGA) module or a plastic ball grid array (PBGA) module..

30. The electronic structure of claim 24, wherein the first substrate includes a semiconductor chip.